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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,145	10/17/2003	Tao Li	030349	9230

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QUALCOMM INCORPORATED
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EXAMINER	
AHN, SAM K	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/08/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/688,145	LI ET AL.	
	Examiner	Art Unit	
	Sam K. Ahn	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see p.8, filed 12/06/06, with respect to the rejection(s) of claim(s) 1,3,4,11,13-16,21,22 and 26 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,11,13-17,20-22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously).

Regarding claim 1, Nakamura teaches an integrated circuit comprising: a despreading unit (201a in Fig.5) operative to despread input samples and provide despread symbols for a first code channel (DPCCH) with a first spreading factor (FIXED SF); a channel compensation unit (201d) operative to multiply the despread symbols with channel estimates and provide demodulated symbols for the first code channel (DPCCH); and a symbol combiner

(201e,201f,207) operative to combine groups of demodulated symbols of the first code channel (input to 201f from $201_1 - 201_n$, further computed for power calculation 207) to obtain recovered data symbols (*output of 202a delivered to the symbol replica interface 205, wherein 205 is coupled to a demodulator 400 in Fig.1 for demodulating the received first and second code channels*) for a second code channel (DPDCH, output of 207 compensating to properly recover for DPDCH) with a second spreading factor (Minimum SF) that is an integer multiple of the first spreading factor (note paragraph 22 and 74 wherein SF_{min} = 4,8,16... wherein the spreading factor is defined by 2^n).

And although Nakamura does not explicitly teach the symbol combiner combining the groups of demodulated symbols for at least two symbol periods of the first code channel, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to recognize from the teaching of Nakamura that the first code channel (DPCCH) with spreading factor higher than minimum spreading factor by integer multiple would have higher number of spreading code per symbol (note paragraph 0074). Spreading factor of 4 holds "1,1,-1,-1" while spreading factor of 8 holds "1,1,-1,-1,1,1,-1,-1". Nakamura further illustrates the first and second code channels synchronously received by frames in figure 2 with different spreading factors for each of the code channels. Hence, one skilled in the art would recognize that in order to properly combine per symbol by the symbol combiner (201e,201f), at least two symbol periods of the first code

channel, for example, with spreading factor of 4 in order to align with the second code channel, for example, with spreading factor of 8.

Applicant has not disclosed that two symbol period provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with other spreading factors for the first and second code channels because the spreading factors can assigned with other numbers as Nakamura teaches in figure 2 of variations. Therefore, it would have been obvious to one of ordinary skill in this art to modify the system of Nakamura by configuring the spreading factors of the two code channels such that at least two symbol periods of the first code channel is combined to obtain the invention as specified in the claim.

Regarding claim 2, Nakamura further teaches wherein the second spreading factor an integer multiple of the first spreading factor (note paragraph 22 and 74 wherein SF_{min} = 4,8,16... wherein the spreading factor is defined by 2^n). And although Nakamura does not explicitly teach wherein the second spreading factor is two times the first spreading factor, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement as such. Applicant has not disclosed that two times the first spreading factor provides an advantage, is used for a particular purpose or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with four or eight times the first spreading factor because the transmitter and the receiver would know which code would be used beforehand (note paragraph 0077). Therefore, it would have been obvious to combine to one of ordinary skill in this art to modify that the relationship between Minimum SF and Fixed SF of Nakamura to be two times the spreading factor to obtain the invention as specified in claim.

Regarding claim 3, Nakamura further teaches wherein the symbol combiner (201e) is operative to combine the groups of demodulated symbols to obtain recovered data symbols for a third code channel (DPDCH) with the second spreading factor (Minimum SF).

Regarding claim 4, Nakamura further teaches wherein the channel compensation unit (201d) is operative to multiply each of the despread symbols with a channel estimate (output of 201b) for one transmitter antenna (1h in Fig.10) to obtain one demodulated symbol (output of 202a or 202b) for the despread symbol.

Regarding claim 11, the claim is rejected as applied to claim 1 with similar scope.
Regarding claim 13, the claim is rejected as applied to claim 1 with similar scope.
Regarding claim 14, the claim is rejected as applied to claim 1 with similar scope.
Regarding claim 15, the claim is rejected as applied to claim 1 with similar scope.

Regarding claim 16, the claim is rejected as applied to claim 1 with similar scope.

Regarding claim 17, the claim is rejected as applied to claim 2 with similar scope.

Regarding claim 20, Nakamura teaches all subject matter claimed, as applied to claim 16. Although Nakamura does not explicitly teach wherein the channel compensation unit and symbol combiner are operated in a pipeline manner, one skilled in the art would analyze that the channel compensation unit (201b) and the symbol combiner (201e,201f) are operating in a pipeline manner, wherein the different channel paths (DPDCH, DPCCH) are operating in parallel for the purpose of maximizing computation capacity and to increase the speed of computation of different channels.

Regarding claim 21, Nakamura further teaches a channel selector (201g) to receive the despread symbols for the plurality of first code channels and provide a despread symbol for one first code channel at a time to the channel compensation unit (201b, note paragraph 0083).

Regarding claim 22, Nakamura further teaches wherein the channel compensation unit (201b) is operative to multiply (201d) despread symbols from the channel selector (201g) with the channel estimates to obtain the demodulated symbols, and wherein the symbol combiner (201f) is operative to combine the demodulated symbols from the channel compensation unit (201b) with accumulated symbols to obtain combine symbols (out of 201f), the

accumulated symbols being indicative of partial combining results for the recovered data symbols and the combined symbols being indicative of updated combining results for the recovered data symbols.

Regarding claim 26, the claim is rejected as applied to claim 1 with similar scope.

3. Claims 5,6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously) and Fitton et al. US 2004/0017843 A1 (Fitton, cited previously).

Regarding claim 6, Nakamura teaches all subject matter claimed, as applied to claim 1. Although Nakamura teaches wherein the channel compensation unit (201d) is operative to multiply each of the despread symbols with channel estimates to obtain two demodulated symbols (output of 202a and 202b) for the despread symbol (processed in 201a), Nakamura does not explicitly teach wherein the symbol combiner is operative to combine groups of demodulated symbols based on space time transmit diversity (STTD) or transmitted using two transmitter antennas.

Fitton teaches channel compensation unit (430 in Fig.4) receiving signal based on space time transmit diversity (STTD, note paragraph 0077) using two transmit antennas (note paragraph 0243).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Fitton in the system of Nakamura by transmitting signals using STTD for the purpose of effectively transmitting

orthogonal data streams, thus reduce the likelihood of losing data due to intersymbol interference (note paragraph 0243).

Regarding claim 5, Fitton further teaches wherein the symbol combiner is operative to combine groups of two demodulated symbols (note paragraph 0243, wherein two symbol periods is required to demodulate two symbols).

Regarding claim 8, the claim is rejected as applied to claim 2 with similar scope.

4. Claims 7,12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously) and Fitton et al. US 2004/0017843 A1 (Fitton, cited previously) and Miyoshi et al. US 2003/0067967 A1 (Miyoshi, cited previously).

Regarding claim 7, Nakamura in view of Fitton teaches all subject matter claimed, as applied to claim 6. However, Nakamura in view of Fitton do not explicitly teach wherein the symbol combiner is operative to combine groups of four demodulated symbols for four symbol periods.

Miyoshi teaches wherein the symbol combiner (503 in Fig. 6) is operative to combine groups of four demodulated symbols for four symbol periods (note paragraph 0043).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Miyoshi in the symbol combiner of

Nakamura for the purpose of properly receiving the signal wherein spreading factor is of four (note paragraph 0043 of Miyoshi), thus obtain the recovered data symbols for the second code channel (DPDCH) of Nakamura.

Regarding claim 12, the claim is rejected as applied to claim 7 with similar scope.

Regarding claim 18, the claim is rejected as applied to claim 7 with similar scope.

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously) in view of Takano et al. US 2005/0277419 A1 (Takano, cited previously).

Regarding claim 9, Nakamura teaches the system employed in a W-CDMA environment implementing DPCCH and DPDCH channels. However, Nakamura does not explicitly teach HS-PDSCH and PDCH channels.

Takano teaches HS-PDSCH and PDCH (DPCH) channels (see Fig.10) of transmission and reception of signals among base stations, mobile station and RNC. Thus, , it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Takano in the system of Nakamura of transmitting and receiving the HS-PDSCH and PDCH channels for the purpose of receiving different signals including HS-PDSCH and PDCH in order to communicate among base stations, mobile station and RNC using the system of Nakamura

Regarding claim 10, the claim is rejected as applied to claim 9 with similar scope.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously) in view of Mazawa et al. US 6,628,631 B1 (Mazawa, cited previously).

   Regarding claim 19, Nakamura teaches all subject matter claimed, as applied to claim 16. However, Nakamura does not explicitly teach wherein the symbol combiner is processed in a time division multiplexed (TDM) manner, one first cod channel at a time.

   Mazawa teaches wherein a symbol combiner (606 in Fig.6) is processed in a time division multiplexed (TDM) manner, one first cod channel at a time (note col.11, lines 24-43, wherein the output of the symbol combiner is coupled to the multiplexer 607 outputting in the TDM manner for each channel). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Mazawa in the system of Nakamura by implementing the multiplexing function after the symbol combiner, thus enabling to share the symbol combiner for plurality of channels, wherein Nakamura also discloses a data and control channels, in order to reduce the number of hardware devices implemented.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously) in view of Boesel et al. US 2004/0071199 A1 (Boesel, cited previously).

Regarding claim 23, Nakamura teaches all subject matter claimed, as applied to claim 22. However, Nakamura does not explicitly teach a symbol buffer operative to provide the accumulated symbols and store the combined symbols.

Boesel teaches a symbol buffer (54 in Fig.7) to provide the accumulated symbols and store the combined symbols (note paragraph 0057). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the symbol buffer coupled to the symbol combiner (201f) of Nakamura for the purpose of correcting rate phase to a desired sub-chip phase by coupling an address generator (52) to the symbol buffer (note paragraph 0057).

8. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. US 2002/0136278 A1 (Nakamura, cited previously) in view of Boesel et al. US 2004/0071199 A1 (Boesel, cited previously) and Bloebaum US 6,295,023 B1 (cited previously).

Regarding claim 24, Nakamura in view of Boesel teach all subject matter claimed, as applied to claim 23. However, Nakamura in view of Boesel do not explicitly teach wherein the symbol buffer includes a first and second memories for first and second code channels.

Bloebaum teaches wherein the symbol buffer (135 in Fig.5) includes first and second memories (symbol buffer arrays, note col.10, lines 1-2) for first and second code channels (Channel 1 and Channel 2). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate

the teaching of Bloebaum in the symbol buffer of Boesel for the purpose of increasing the flexibility of the symbol buffer by providing variable controllable delays to the symbol buffer, which is well-known to one skilled in the art. Furthermore, it would have been obvious to one skilled in the art at the time of the invention to access alternately between the first and second memory banks controlled by a multiplexer (well-known function to one skilled in the art) as each channel may not have data to demodulate at all times, thus need to be accessed only when needed for the purpose of reducing overall processing of the system by accessing the memory banks only when required.

Regarding claim 25, the claim is rejected as applied to claim 24 with similar scope.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
Patent Examiner
1/3/07